HIGH-SPEED TEST

(Loop)back to the future

New test methods tackle ≥6.4Gbps data rates

*Manufacturers of microprocessors and high-end graphics chipsets are now employing high-speed serial buses like PCI Express and HyperTransport to deliver data and I/O rates up to 6.4Gbps. By 2010, 10Gbps and above may be the norm.**

Test, as always, will play a critical role in delivering these exponentially higher speeds at not-much-higher cost. However, faster serial buses introduce tough challenges, where traditional functional test and simple design-for-test (DFT) methodologies fall short. Older "functional" test flows on high-end ATE platforms offer the most thorough fault coverage, but these time-tested methods prove increasingly prohibitive in terms of cost, complexity and cycle times. Moreover, cost per pin rises with bus speed in high-speed data applications, making functional testing even less viable.

Manufacturers have thus turned to loopback techniques (i.e., using the device to source the test data and receive it back into the device for recognition) that enable cost optimized testing of today's high-speed buses. Loopback testing can be very effective, but the manner in which it is implemented is especially critical, considering the typical loss budget for high-speed signals. This loss budget, which determines the magnitude of acceptable signal degradation, typically has three components—contributed by the transmitter, receiver, and interconnect—all of which could degrade the signal "eye" over the loopback path and thus impact coverage.

To date, alternative DFT techniques like "near-end loopback" have already introduced cost efficiencies (via ease of programming and reduced capital investment in ATE) in testing devices for high-end consumer and computing applications. Near-end loopback techniques can be self-contained within the DUT with pathways created between the I/O pins. However, the inherent cost savings and simplicity carry stiff tradeoffs in terms of coverage. There are no parametric measurements, a lack of signal control, and lower likelihood of catching faults related to signal integrity or bit errors. For example, a simple internal, or load board loopback, would allow a marginal receiver to "hide" in the shadow of a robust transmitter and pass the loopback test screen. While these uncertainties can be worked around at lower speeds, compromising coverage at ≥6.4Gbps is way too risky.

Far-end Loopback: Less Jittery, Lower Cost

Between the two extremes, innovative techniques such as far-end loopback combine the flexibility of DFT with the more in-depth diagnostics of functional testing. Lengthening the feedback path by placing the DUT in communication with an intelligent but still cost-effective tester makes production-level testing of high-speed buses viable for the first time. Even more compelling, far end loopback with programmable signal degradation can be employed to cut costs and speed time-to-market while introducing unprecedented coverage.

This type of loopback offers significant advantages:

- Provides signal control to stress the eye
- Increased coverage in detecting sensitivity to signal integrity issues and bit errors
- Addition of circuitry enabling jitter to be injected and measured
- Covers all three parts of the loss budget
- R_X and T_X channels can be used to deliver test vectors to the core logic and protocol stack
- Access to device pins for full DC parametric testing

Clearly, exponentially faster bus speeds are driving fundamental shifts across the board, from design through production. Test companies can play an important leadership role in this fast-paced environment, by delivering innovative products and solutions that enable customers to optimize and accelerate their latest test methodologies at lower cost, while minimizing risk.

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*ITRS 2005 Roadmap